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Relevance scale ☐ ☐ ☐ ☐ ☐**1** [A perceptually-supported sketch editor](#)

Eric Saund, Thomas P. Moran

November 1994 **Proceedings of the 7th annual ACM symposium on User interface software and technology**Full text available: [pdf\(798.89 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The human visual system makes a great deal more of images than the elemental marks on a surface. In the course of viewing, creating, or editing a picture, we actively construct a host of visual structures and relationships as components of sensible interpretations. This paper shows how some of these computational processes can be incorporated into perceptually-supported image editing tools, enabling machines to better engage users at the level of their own percepts. We focu ...

Keywords: PerSketch, computer vision, drawing tools, gestures, graphics editing, image editing, interactive graphics, machine vision, pen computing, perceptual grouping, perceptual organization, scale space blackboard WYSIWYG, sketch tools, token grouping

**2** [Octrees for faster isosurface generation](#)

Jane Wilhelms, Allen Van Gelder

July 1992 **ACM Transactions on Graphics (TOG)**, Volume 11 Issue 3Full text available: [pdf\(5.16 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

The large size of many volume data sets often prevents visualization algorithms from providing interactive rendering. The use of hierarchical data structures can ameliorate this problem by storing summary information to prevent useless exploration of regions of little or no current interest within the volume. This paper discusses research into the use of the octree hierarchical data structure when the regions of current interest can vary during the applicat ...

Keywords: hierarchical spatial enumeration, isosurface extraction, octree, scientific visualization

**3** [A Framework for Sample-Based Rendering with O-Buffers](#)

Huamin Qu, Arie Kaufman, Ran Shao, Ankush Kumar

October 2003 **Proceedings of the 14th IEEE Visualization 2003 (VIS'03) VIS '03**Full text available: [pdf\(281.77 KB\)](#) Additional Information: [full citation](#), [abstract](#)

We present an innovative modeling and rendering primitive, called the O-buffer, for sample-based graphics, such as images, volumes, and points. The 2D or 3D O-buffer is in essence a


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61 [Processor frequency setting for energy minimization of streaming multimedia application](#)

Andrea Acquaviva, Luca Benini, Bruno Riccò

 April 2001 **Proceedings of the ninth international symposium on Hardware/software codesign**

 Full text available: pdf(401.70 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

In this paper, we describe a software-controlled approach for adaptively minimizing energy in embedded systems for realtime multimedia processing. Energy is optimized by clock speed setting: the software controller dynamically adjusts processor clock speed to the frame rate requirements of the incoming multimedia stream. The speed-setting policy is based on a system model that correlates clock speed with best-case, average-case and worst-case sustainable frame rate, accounting for data-depend ...

62 [CMOS VCOs for frequency synthesis in wireless biotelemetry](#)

Rafael J. Betancourt-Zamora, Thomas H. Lee

 August 1998 **Proceedings of the 1998 international symposium on Low power electronics and design**

 Full text available: pdf(324.97 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

A new phase noise model was used to optimize a differential ring VCO for minimum power consumption. We compare the phase noise performance of three buffer stages using clamped, symmetric and cross-coupled loads, respectively. We propose a cross-coupled buffer topology that achieves lower phase noise by exploiting symmetry. Measured phase noise for a 1.2mW, 150MHz VCO fabricated in 0.5μm CMOS is -103.9dBc/Hz at 500KHz offset, showing good agreement with the theory.

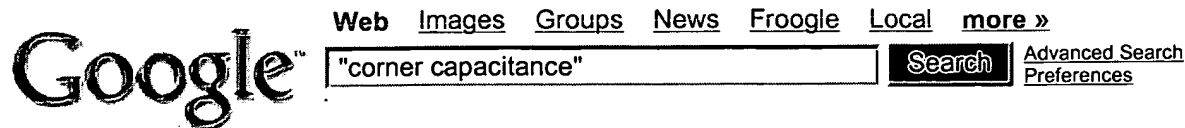
63 [Low Power Design: Power and CAD considerations for the 1.75mbyte, 1.2ghz L2 cache on the alpha 21364 CPU](#)

Joel Grodstein, Rachid Rayess, Tad Truex, Linda Shattuck, Sue Lowell, Dan Bailey, David Bertucci, Gabriel Bischoff, Daniel Dever, Mike Gowan, Roy Lane, Brian Lilly, Krishna Nagalla, Rahul Shah, Emily Shriver, Shi-Huang Yin, Shannon Morton

 April 2002 **Proceedings of the 12th ACM Great Lakes symposium on VLSI**

 Full text available: pdf(205.76 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

A 1.75 MByte L2 cache has been designed and fabricated as part of the Alpha 21364 microprocessor[1] (Figure 1), in a .18m bulk CMOS process. The cache was designed to run at 1.2 GHz, and pass-1 samples confirm this. While Alpha CPUs are known primarily for high speed, the combination of package constraints and a tight schedule forced careful attention to the integrated whole of power expenditure and the interaction of CAD with design. The cache consumes only 7% of total die power.



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